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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,972	12/13/2001	Edward P. Kuzemchak	TI-32964	7240

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EXAMINER

CHOW, CHIH CHING

ART UNIT	PAPER NUMBER
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2192

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/022,972	Applicant(s) KUZEMCHAK ET AL.	
	Examiner Chih-Ching Chow	Art Unit 2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2004.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1 and 2 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 29 December 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 1/21/05.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>07/25/02</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. This action is responsive to amendment dated December 29, 2004.
2. Per Applicants' request, claims 1 and 2 have been amended.
3. Claims 1-2 remain pending.

Response to Amendment

4. Applicants' amendment dated 12/29/2004, responding to the 10/20/2004 Office action provided in the rejection of claims 1 and 2. The examiner has reviewed the updated specification. Claims 1-2 remain pending.
5. Applicants' amendment dated 12/29/2004, responding to the 10/20/2004 Office action provided in the objection of drawings. The examiner has reviewed the updated drawings respectfully.
6. The set of formal drawings filed concurrently with the above-mentioned amendment is accepted by the Examiner.
7. Applicants' amendment dated 12/29/2004, responding to the 10/20/2004 Office action provided in the objection of specification. The examiner has reviewed the updated specification respectfully.
8. The objection to the specification is hereby withdrawn in view of Applicants' amendment to the specification.
9. Applicants' Foreign Priority document filed on 01/21/2005, responding to the 10/20/2004 Office action provided in the objection of Priority. The examiner has reviewed the filed Foreign Priority document respectfully.
10. The objection to the priority is hereby withdrawn in view of Applicants' Foreign Priority document.

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11. Applicants' Oath and Declaration document filed on 01/21/2005, responding to the 10/20/2004 Office action provided in the objection of undersigned Declaration. The examiner has reviewed the filed Oath and Declaration document respectfully.
12. The objection to the priority is hereby withdrawn in view of Applicants' Oath and Declaration document.
13. The Examiner is maintaining the Double Patenting rejection to the copending application S.N. 10/017,777, since the Applicant has not submitted a terminal disclaimer to obviate the basis of the rejection.

Response to Arguments

14. Applicants' arguments for Claims 1-2 have been fully considered respectfully by the examiner but they are not persuasive.
15. Applicants' arguments are basically in the following points:
 - The combined teaching of Laurenti and Gerra fall short of the requirement of claim 1.

Examiner's Response: In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Laurenti's disclosure teaches general microprocessor architecture, DSP (Digital Signal Processing), and execution of pipelined instructions. Gerra's disclosure teaches DSP modeling and integrating HW and SW verifications. It's obvious to one of ordinary skill in the art, to use microinstruction processing taught by Laurenti, supplement with Gerra's simulation model also used for pipeline structured

microinstruction processing, see Gerra's Abstract, "Our models have been integrated into a number of cycle-based and event-driven system simulation environments. We present one such experience in incorporating these models into a VHDL environment. The accuracy has been verified cycle-by-cycle against the gatdRTL level models." And Gerra's page 964, 5th paragraph, "logic. For these types of processors, bus interface models become very complex, and must include modeling of pipeline and architecture information in order to recover the necessary timing."

- Claim 1's effective addresses calculations is not disclosed in Guerra's citation.

Examiner's Response: In response to applicant's argument that Guerra is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Guerra teaches a DSP modeling using a pipeline structure. Basically, it compares two program's execution cycles, and the cycle calculation is related to the effective address calculation. It 'calculates' the microinstruction's delays, latencies calculation, clock cycle synchronizations, etc. Even it does not specifically mentioned 'effective address', it's well know to the people in the art that the effective address is the actual address of data or an instruction in main storage, which is going to take place for the next clock cycle - therefore the figure 2 and 3 have shown the capability of determining, calculating, computing, and reporting of effective address as claimed in current application.

- Claim 2 is rejected under 35 USC 103 and why items (b) and (c) may be allowable?

Examiner's Response: The claim 2 (b) and (c) specifically mentions the 'steps of finding the current address delay, and computing the current effective address delay'. If the actual step is disclosed and that adds limitation to the 'calculation' and 'computing', it might be considered to be allowable. -- however Applicants have never disclose the details of it.

16. Examiner is maintaining the Double Patenting and the 35 USC 103

Rejections. For the Applicants' convenience they are listed as following, with the amendments requested by the Applicants.

Double Patenting

17. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

18. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 10 of copending Application No.10/017,777. Although the conflicting claims are not identical, they are not patentably distinct from each other, from the comparison listed in the following table:

Current Application (10/022,972) US 2003/0088855A1	Co-Application (10/017,777) US 2002/0184613A1
Claim 1	Claim 10
A method for determining in software the effective address of instructions in a program executed on a pipelined architecture where there is no external visibility into the pipeline, the method comprising the steps of:	A method for verifying that two programs are equivalent, the method comprising the steps of:
executing a first program	executing a first program
	collecting a first set of events ...
	executing a second program
	collecting a second set of events ...
	determining if the first set of events is equivalent to the second set of events by reconciling the first set of events and the second set of events

	indicating the first program is not equivalent to the second program if an unreconciled event is discovered during the step of determining
determining that a first instruction is in the pipeline	determining that a first instruction is in the <i>instruction</i> pipeline
calculating the current effective address delay of the instruction in the pipeline	calculating the current effective address delay of the instruction in the pipeline
Determining whether a valid effective address for the instruction is available based on the current effective address delay of the instruction	finding that a valid effective address for the instruction is available based on the current effective address delay of the instruction
computing the effective address of the instruction responsive to determining that a valid effective address is not available; and	computing the effective address of the <i>first</i> instruction if a valid effective address is not available; and
reporting the effective address of the instruction	reporting the effective address of the instruction

Claim 1 of current application is anticipated by co-application claim 10 in that co-application claim 10 contains all the limitations of the current application claim 1. Claim 1 of the current application therefore is not patentably distinct from co-application claim 10 and as such is unpatentable for obvious-type double patenting.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

19. Claim 2 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 12 of copending Application No.10/017,777. Although the conflicting claims are not

identical, they are not patentably distinct from each other for the same reasons since the claim 2 of current application inherited the features of claim 1.

Current Application (10/022,972) US 2003/0088855A1	Co-Application (10/017,777) US 2002/0184613A1
Claim 2	Claim 12
The method of Claim 1 wherein:	The method of Claim 11 wherein:
the step of calculating comprises subtracting the number of clock cycles that have occurred since the instruction entered the pipeline from the number of clock cycles required to compute the effective address of the instruction;	the step of calculating comprises subtracting the number of clock cycles that have occurred since the instruction entered the pipeline from the number of clock cycles required to compute the effective address of the instruction
wherein the determining step comprises determining whether the current effective address delay is 0 ; and	the step of finding comprises determining that the current effective address delay is 0; and
wherein the step of computing is executed responsive to the current effective address delay being less than 0.	the step of computing is executed if the current effective address delay is less than 0

Claim 2 of current application is anticipated by co-application claim 12 in that co-application claim 12 contains all the limitations of the current application claim 2. Claim 2 of the current application therefore is not patentably distinct from co-application claim 12 and as such is unpatentable for obvious-type double patenting.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

21. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,658,578 by Gilbert Laurenti et al. (hereinafter "Laurenti"), in view of Guerra et al., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification", 1999-ACM.

CLAIM

1. A method for determining in software the effective address of instructions in a program executed on a pipelined architecture where there is no external visibility into the pipeline, the method comprising the steps of:

Laurenti / Guerra

Laurenti teaches the feature of determining the effective address of instructions in a program executed on a pipelined architecture, in Laurenti's Abstract, "The processor includes a **multistage execution pipeline with pipeline protection features.**", in Laurenti, column 28, lines 20-15, "On the processor device, when accessing long words in memory, the **effective address** is the address of the most significant word (MSW) of the 32-bit data. The address of the least significant word (LSW) of the 32-bit data is: At the next address if the effective address is even. Or at the previous address if the effective address is odd." Laurenti also teaches 'no external visibility into the pipeline' feature. In Laurenti, column 65, "AVIS Address visibility mode AVIS = 0 The external address lines do not change with the internal program address. (*no external visibility into the pipeline*). Control and data lines are not

- (a) executing a first program;
- (b) determining that a first instruction is in the pipeline;
- (c) calculating the current effective address delay of the instruction in the pipeline;
- (d) determining whether a valid effective address for the instruction is available based on the current effective address delay of the instruction;
- (e) computing the effective address of the instruction responsive to determining that a valid effective address is not available; and
- (f) reporting the effective address of the instruction.

affected and the address bus is driven with the last address on the bus. (See **pipeline protection note**", further, in column 159, lines 46-51, "During normal operation the addresses for internal devices will **not be output on the external bus** in order to conserve power. Normally when in AVIS mode the cache controller will be disabled to guarantee that external program bus slots are always available." Laurenti teaches the *determining effective address of instructions in a program executed on a pipelined architecture with no external visibility into the pipeline* but does not teach items a-f specifically. However Guerra teaches those features in an analogous prior art. In Guerra, page 966, section 2.3, Figure 2 and Figure 3, showing the capability to determine, calculate, compute, and report of instruction delay as claimed. Guerra recites the modeling was done in a pipelined architecture, on page 966, last paragraph, "Consider the example shown in Figure 3 for a different 5-stage **pipeline**." It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Laurenti's disclosure of the pipelined architecture by the statistical traces taught by Guerra for the purpose of modeling and integration of pipelined architecture (see Guerra Abstract).

2. The method of Claim 1 wherein:

(a) the step of calculating comprises subtracting the number of clock cycles that have occurred since the instruction entered the pipeline from the number of clock cycles required to compute the effective address of the instruction;

(b) wherein the determining step comprises determining whether the current effective address delay is 0 ; and

(c) wherein the step of computing is executed responsive to the current effective address delay is less than 0.

For the feature of claim 1 see claim 1 rejection. In Guerra, section 2.2, 2nd paragraph, "The co-verification model consists of the ISA simulator and a Bus Interface Model, BIM (Figure 1a). The interface model itself is also partitioned into two parts, the bus pin model and the bus cycle scheduler. The latter collects the information about the software events, identifies the corresponding hardware events, and schedules them in proper order for each clock cycle." The clock cycles calculation feature is specified there.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Ching Chow whose telephone number is 571-272-3693. The examiner can normally be reached on 7:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature of relating to the status of this application should be directed to the **TC2100 Group receptionist: 571-272-2100.**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chih-Ching Chow

Examiner

Art Unit 2192

April 14, 2005

Hoangin Antony Nguyen Ba

CC

ANTONY NGUYEN-BA
PRIMARY EXAMINER